PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Commissioner
US Department of Commerce
United States Patent and Trademark
Office, PCT
2011 South Clark Place Room
CP2/5C24
Arlington, VA 22202
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 30 July 2001 (30.07.01)	
International application No. PCT/US00/28059	**Applicant's or agent's file reference** RCA 89265
International filing date (day/month/year) 11 October 2000 (11.10.00)	**Priority date** (day/month/year) 13 October 1999 (13.10.99)
Applicant CARLSGAARD, Eric, Stephen et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

02 May 2001 (02.05.01)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No.: (41-22) 740.14.35	Authorized officer Zakaria EL KHODARY Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
RCA 89265		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 00/ 28059	11/10/2000	13/10/1999
Applicant		
THOMSON LICENSING S.A.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 2

   [X] as suggested by the applicant.

   [ ] None of the figures.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/28059

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N9/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal

C DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 98 46027 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 15 October 1998 (1998-10-15) page 1, line 6 - line 18 page 3, line 16 -page 4, line 9 ---	1-6,9-13
A	US 5 367 337 A (PYLE HARRY S ET AL) 22 November 1994 (1994-11-22) column 2, line 16 - line 34 column 4, line 14 - line 30 column 9, line 20 -column 10, line 15 ---	1-6
A	WO 99 46931 A (GEN INSTRUMENT CORP) 16 September 1999 (1999-09-16) page 5, line 5 - line 18 page 6, line 26 -page 7, line 14 page 21, line 1 - line 18 page 26, line 4 -page 27, line 3 ---	1,9,15

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 February 2001	08/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Berwitz, P

Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
PCT/US 00/28059

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 808 691 A (MALCOLM JR RONALD D ET AL) 15 September 1998 (1998-09-15) column 1, line 21 - line 31	1,15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/28059

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9846027 A	15-10-1998	EP 0906701 A	07-04-1999
		JP 2000511747 T	05-09-2000
		US 6064446 A	16-05-2000
US 5367337 A	22-11-1994	NONE	
WO 9946931 A	16-09-1999	US 6147713 A	14-11-2000
		AU 2796099 A	27-09-1999
		EP 1062806 A	27-12-2000
US 5808691 A	15-09-1998	US 6052152 A	18-04-2000

PATENT COOPERATION TREATY

EXPRESS EV025963025US

PPL

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

TRIPOLI, J.
THOMSON MULTIMEDIA LICENSING INC.
P.O. Box 5312
Princeton, New Jersey 08540
ETATS-UNIS D'AMERIQUE

RECEIVED
JAN 31 2002
IS&S

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT
(PCT Rule 71.1)

	Date of mailing *(day/month/year)* 23.01.2002
Applicant's or agent's file reference RCA 89265	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US00/28059	11/10/2000	13/10/1999

Applicant
THOMSON LICENSING S.A. et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Event	Voi Amend Final Claim Selection
Deadline	13 Feb 2002 to Davida
Entered	DPF 2/1/02

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Schalinatus, D Tel.+49 89 2399-8242

In the latter case, however, the main channel is locked to a parameter of the incoming analog television signal, such as horizontal sync pulses or color burst.

WO 98/46027 discloses a multi-standard color decoder system that includes one external asynchronous crystal clock to demodulate all the variants of the PAL/NTSC color system, without digitizing the analog chrominance signal. In a disclosed method of demodulating an analog chrominance signal, digital quadrature signals are generated for demodulating the analog chrominance signal to obtain analog demodulated color difference signals. A digital phase error signal is furnished from at least of the analog demodulated color difference signals. The digital phase error signal is digitally filtered to obtain a phase control signal for the digital quadrature signals generation.

US Pat. No. 5,367,337 discloses an apparatus and method for receiving and sampling an incoming video image signal asynchronously, and then processing the signal to recover the video image, including the video format, for conversion to a preselected video format. The patent discloses oversampling in processing to detect the video format.

US Pat. No. 5,808,691 discloses an apparatus for synthesizing a periodic digital signal having a frequency that is specified by the frequency of a periodic reference signal that is asynchronous with respect to a sampling clock of the periodic digital signal. In a preferred embodiment, a digital video system synthesizes a digital color subcarrier and synchronized to a reference frequency of a crystal oscillator that is asynchronous with respect to a digital system clock for the digital video system.

The present invention is a single system IC that performs simultaneous digitization and processing of multiple analog and/or digital signals, using a common frequency source that is not locked to a parameter of the incoming signal. Thus, high performance sampling and processing of all incoming signals may be achieved.

The present invention provides for standard analog video decoding for two channels using a single reference frequency (reference clock) that is not locked to either system. That is, the reference clock is not based on, or locked to, a lockable characteristic of either input signal. Two digital signal processors, for satellite and terrestrial television signals, are modified to perform processing based on the same reference frequency. The present invention provides synchronous frequency

operation of all A/Ds and digital signal processors of the multiple channels to prevent erroneous sampling and processing of the incoming signal.

In one form of the invention, a single reference clock of a particular frequency is input to a clock generator that generates all of the operational frequencies (clock signals) needed by the A/D converters and decoding circuitry/logic on the IC. The reference clock is independent, e.g., is not locked to, any synchronizing characteristic of the input signals.

Since there is only one reference clock from which all the other sampling and processing frequencies are generated, the A/Ds will be able to operate with high performance, up to 10-bit accuracy, with little to no digital noise. This is generally not possible with asynchronous sampling frequencies because "quiet zones", needed for sampling the analog input, no longer exist. However, with the multiple sampling frequencies based on a single reference clock (frequency) of the present invention, these quiet zones between digital transitions are preserved.

One circuitry/logic section of the present IC that processes satellite (digital) broadcast television signals, uses an interpolator to process an incoming signal at an appropriate symbol rate related frequency (e.g. 40 MHz) even though

CLAIMS

1. A signal processing apparatus, comprising:

a signal input for receiving an analog signal having a synchronizing characteristic;

a first clock generator for generating a reference clock signal, the reference clock signal being independent of the synchronizing characteristic of the analog signal;

a second clock generator, coupled to the first clock generator, for producing a plurality of further clock signals in response to the reference clock signal; and

a signal processing section, coupled to the signal input and the second clock generator, for sampling and processing the analog signal in accordance with a sampling rate and an appropriate signal standard, the signal processing section having a plurality of analog to digital (A/D) converters that are clocked by respective ones of the plurality of further clock signals, characterized in that

the A/D converters are clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing characteristic of the input analog signal and have a frequency substantially equal to the sampling rate, whereby corruption of the analog signal by digital noise in the apparatus is prevented.

2. The signal processing apparatus of claim 1, characterized in that the signal processing section is adapted to process two separate analog signals, each of the two separate analog signals having respective synchronizing characteristics, and the reference clock signal is independent of both of the synchronizing characteristics.

3. The signal processing apparatus of claim 2, characterized in that the signal processing section processes the two separate analog signals using a single processing channel, the single processing channel being clocked by a further clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the analog signals.

4. The signal processing apparatus of claim 3, characterized in that the analog signals are television signals.

5. The signal processing apparatus of claim 1, characterized in that the signal processing section is further operable to process a digital input signal having a synchronizing characteristic, and the reference clock signal is independent of the synchronizing characteristic of the digital input signal.

6. A television apparatus, comprising:

a signal input for receiving a television signal having a synchronizing characteristic;

a first clock signal generator for producing a reference clock signal that is independent of the synchronizing characteristic of the television signal;

a second clock signal generator, coupled to the first clock signal generator, for producing a plurality of further clock signals in response to the reference clock signal;

a signal processor, coupled to the signal input and the second clock signal generator, for sampling and processing the input signal in accordance with an appropriate signal standard and providing an output signal suitable for display on a display device, the signal processor including a plurality of analog to digital (A/D) converters coupled to the second clock signal generator; and

an signal output, coupled to the signal processor, for receiving and coupling the output signal to a display device, characterized in that

the A/D converters of the signal processor are clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing characteristic of the input signal, and have a frequency substantially equal to the sampling rate whereby corruption of the analog signal by digital noise in the apparatus is prevented.

7. The television apparatus of claim 6, characterized in that the signal processing section is adapted to process two separate analog signals, each of the two separate analog signals having respective synchronizing characteristics, and the reference clock signal is independent of the synchronizing characteristics.

8. The television apparatus of claim 7, characterized in that the analog signal processing section processes the two separate analog signals using a single processing channel, and the single processing channel is clocked by an internal clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the analog signals.

9. A method for processing input signals having synchronizing components, the method comprising the steps of:

receiving an input signal having a synchronizing component;

generating a reference clock signal, the reference clock signal being independent of the synchronizing characteristic of the input signal;

generating a plurality of further clock signals based on the reference clock signal;

converting the analog input signal into a digital signal using analog to digital (A/D) converters that are clocked using one of the plurality of further clock signals; and

decoding the converted digital signal in accordance with an appropriate television signal standard using decoding circuitry/logic to provide an output signal suitable for display, the decoding circuitry/logic being clocked by at least one of the plurality of further clock signals, characterized in that

the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing characteristic of the input signal and have a frequency substantially equal to the sampling rate whereby corruption of the analog signal by digital noise is prevented.

10. The method according to claim 9, characterized in that

the receiving step comprises receiving two analog input signals, each having a respective synchronizing characteristic,

the converting step comprises converting the two analog input signals to respective digital signals, and

the decoding step comprises decoding the two digital signals to provide two output signal using a single processing channel that is clocked by an internal clock signals that has a frequency of at least twice the required clocking speed necessary for processing a single analog signal.

11. The method according to claim 9, characterized in that

the receiving step further comprises receiving a digital input signal having a synchronizing characteristic, and

the decoding step further comprises decoding the digital input signal using decoding circuitry/logic that is clocked by a respective one of the internal clock signals that is independent of the synchronizing characteristic of the digital input signal.

12. The method according to claim 9, characterized in that

the receiving step comprises receiving an analog television signal.

PATENT COOPERATION TREATY

PCT

REC'D 25 JAN 2002
WIPO PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
RCA 89265		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US00/28059	11/10/2000	13/10/1999
International Patent Classification (IPC) or national classification and IPC H04N9/66		
Applicant THOMSON LICENSING S.A. et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 6 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
02/05/2001	23.01.2002
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Loeser, E Telephone No. +49 89 2399 8482

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/US00/28059

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

1,3-13	as originally filed			
2,2a	as received on	13/12/2001	with letter of	10/12/2001

Claims, No.:

1-12	as received on	13/12/2001	with letter of	10/12/2001

Drawings, sheets:

1-5	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-12
	No:	Claims	
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-12
Industrial applicability (IA)	Yes:	Claims	1-12
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

1. General

The following documents are cited:
D1: WO-A-98/46027;
D2: US-A-5 367 337;
D3: US-A-5 808 691.

The claims do not satisfy the criteria set forth in Articles 6 and 33(3) PCT. Details of the objections are set out below.

2. Claim 1: Art. 6 PCT and Art. 33(3) PCT

2.1.

Claim 1 effectively specifies

a **signal processing apparatus** comprising:

(a) a **signal input** for receiving an analog signal having a synchronising characteristic;

(b) a **first clock generator** (50) for generating a reference clock signal,

(b1) the reference clock signal being independent of the synchronising characteristic of the analog signal;

(c) a **second clock generator** (54)

(c1) coupled to the first clock generator

(c2) for producing a plurality of further clock signals in response to the reference clock signal;

(d) a **signal processing section**

(d1) coupled to the signal input and the second clock generator

(d2) having a plurality of A/D converters

(d3) that are clocked by respective ones of the plurality of further clock signals

(d4) for sampling and processing the analog signal in accordance with a sampling rate and an appropriate signal standard;

(e) the frequencies of the plural further clock signals are substantially equal to the sampling rates of the A/D converters

(e1) **whereby/so that** corruption of the analog signal by digital noise in the apparatus is prevented.

2.2.

It is accepted that using synchronised stable clocks in the apparatus and sampling the analog input signal may help in preventing corruption of the analog signal. This would be obtained by using mutually synchronised clocks whose well-known noise caused by transients of the clock signals would be concentrated in predefined synchronised time intervals while some time intervals between the former intervals would be free of transient noise.

Accordingly, it would be required to sample the input signal at a phase relative to the sampling clock that is not affected by the aforementioned noise.

Feature (e1) is drafted in terms of a result to be obtained. The claim fails to define the means required to obtain the desired effect, ie the means that assure that the sampling phase is controlled such by sampling solely in "quite zones" (p. 11 line 5) which exclude the periods of transient noise caused by the synchronised clocks. Such a feature considered essential to the invention is presently missing.

In this context, it is noted that due to processing delays in a signal processing circuit, the time intervals in which noise by clock transients will occur may be quite large. Further, other sources of noise due to other digital processing steps may corrupt the analog signal prior to sampling.

It is considered difficult to obtain the claimed result of effectively fully preventing any corruption of the analog signal. Present claim 1 fails to define the means required to obtain that result.

The claim specifies plural A/D converters respectively operating at a sampling clock substantially equal to one of the plural clock frequencies. However, for a signal analog signal to be converted, a single converter would suffice. Thus it is not clear for which purpose the other converters are provided, and how they are technically related to the conversion of the single analog input signal.

For these reasons claim 1 contravenes Art. 6 PCT.

2.3.

D2 (abstract; col.2 lines 16-34; Fig. 5 and col.9 line 20 to col.10 line 15) anticipates at least claimed features (a), (b), (b1), (c), (c1), (c2), (d), (d1), (d4) identified above.

Claim 1 specifies in features (d2),(d3) and (e) a plurality of A/D converters clocked by producing respective ones of the plural further clock signals whose frequencies are substantially equal to the respective ones of the plural clock frequencies. However, only a single input signal is effectively A/D converted.

D2 discloses an apparatus having a single A/D converter clocked by a single further clock signal whose frequency is equal to the converter's sampling rate. The sampling rate is such as to oversample the input signal. The known apparatus, like the apparatus of claim 1, enables sampling during the aforementioned "quiet zones" due its generated clock signals being mutually synchronised and independent of the input signal.

The subject-matter of claim 1 distinguishes from the disclosure of D1 merely by providing further A/D converters that use sampling clock signals that are also synchronised with a common reference frequency.

Such a distinctive feature justifies acknowledgement of novelty, but cannot be considered to establish an inventive step. This is because a skilled person attempting to routinely extend the concept disclosed in D2 would consider providing further A/D converters as required and would consider applying sampling clocks thereto in the same manner as is done for the first converter, ie using clock signals that are derived from, and synchronised to, a common reference clock.

3. Claim 6: Art. 6 PCT and Art. 33(3) PCT

The large degree of overlap between the features of claim 6 with those of claim 1 causes contravention of Art. 6 PCT for lacking conciseness. The few features by which claim 6 distinguishes

from claim 1 could be redrafted without any difficulty in a dependent claim.

Moreover, the substance of the claimed features corresponding to that of claim 1, the objections raised in section 2 above against claim 1 correspondingly apply to claim 6.

4. Claim 9: Art. 6 PCT and Art. 33(3) PCT

The substance of the claimed features corresponding to that of claim 1, the objections raised in section 2 above against claim 1 correspondingly apply to claim 6.

5. Dependent claims and further comments

5.1.
The feature of claim 3, "... process two separate analog signals using a single processing channel ..." is considered to lack support by the description because it appears (Fig.2 Block 86) that a signal processing channel is solely established for to digitized analog, thus digital, signals. The same objection applies to claim 8.

5.2.
The additional features of each of the dependent claims are considered as not being capable of establishing an inventive step. This is because these features are considered obvious design options of a skilled person routinely attempting to implement design alternatives based on the design known from D2.

5.3.
It is to be noted that applying a stable sampling clock, that is independent from any characteristics of the input signal, to a sampling clock input of an A/D converter corresponds to standard technical knowledge.

Moreover, it is generally known in the art to derive from a first stable clock signal a plural number of stable/synchronised

clock signals for application in various portions of a system, as required, as is evident from D2 and, e.g., D1 (p.4 line 27).

It is further considered that the disclosure of D3 (cf eg abstract; Fig.2 and related text passages; col.1 line 21 - col.3 line 34) in combination with the normal design options of the skilled person would also render obvious any of the claimed feature combination.

6. Description and/or formal belongings

6.1. The claims are not complemented with reference signs as required by Rule 6.2(b) PCT.

6.2. A document reflecting the prior art described on page 1 is not identified in the description (Rule 5.1(a)(ii) PCT).

6.3. The summary of relevant document D2 provided on page 2 of the description fails to mention those features in the disclosure of D2 which anticipate the majority of features of the each of the independent claims (cf section 2.1 above).

6.4. The vague statement on page 12 (lines 25-26) referring to a spirit of the invention casts doubt upon the claims' intended scope of protection and should thus be cancelled.

In the latter case, however, the main channel is locked to a parameter of the incoming analog television signal, such as horizontal sync pulses or color burst.

WO 98/46027 discloses a multi-standard color decoder system that includes one external asynchronous crystal clock to demodulate all the variants of the PAL/NTSC color system, without digitizing the analog chrominance signal. In a disclosed method of demodulating an analog chrominance signal, digital quadrature signals are generated for demodulating the analog chrominance signal to obtain analog demodulated color difference signals. A digital phase error signal is furnished from at least of the analog demodulated color difference signals. The digital phase error signal is digitally filtered to obtain a phase control signal for the digital quadrature signals generation.

US Pat. No. 5,367,337 discloses an apparatus and method for receiving and sampling an incoming video image signal asynchronously, and then processing the signal to recover the video image, including the video format, for conversion to a preselected video format. The patent discloses oversampling in processing to detect the video format.

US Pat. No. 5,808,691 discloses an apparatus for synthesizing a periodic digital signal having a frequency that is specified by the frequency of a periodic reference signal that is asynchronous with respect to a sampling clock of the periodic digital signal. In a preferred embodiment, a digital video system synthesizes a digital color subcarrier and synchronized to a reference frequency of a crystal oscillator that is asynchronous with respect to a digital system clock for the digital video system.

The present invention is a single system IC that performs simultaneous digitization and processing of multiple analog and/or digital signals, using a common frequency source that is not locked to a parameter of the incoming signal. Thus, high performance sampling and processing of all incoming signals may be achieved.

The present invention provides for standard analog video decoding for two channels using a single reference frequency (reference clock) that is not locked to either system. That is, the reference clock is not based on, or locked to, a lockable characteristic of either input signal. Two digital signal processors, for satellite and terrestrial television signals, are modified to perform processing based on the same reference frequency. The present invention provides synchronous frequency

operation of all A/Ds and digital signal processors of the multiple channels to prevent erroneous sampling and processing of the incoming signal.

In one form of the invention, a single reference clock of a particular frequency is input to a clock generator that generates all of the operational frequencies (clock signals) needed by the A/D converters and decoding circuitry/logic on the IC. The reference clock is independent, e.g., is not locked to, any synchronizing characteristic of the input signals.

Since there is only one reference clock from which all the other sampling and processing frequencies are generated, the A/Ds will be able to operate with high performance, up to 10-bit accuracy, with little to no digital noise. This is generally not possible with asynchronous sampling frequencies because "quiet zones", needed for sampling the analog input, no longer exist. However, with the multiple sampling frequencies based on a single reference clock (frequency) of the present invention, these quiet zones between digital transitions are preserved.

One circuitry/logic section of the present IC that processes satellite (digital) broadcast television signals, uses an interpolator to process an incoming signal at an appropriate symbol rate related frequency (e.g. 40 MHz) even though

DIGITAL AND ANALOG TELEVISION SIGNAL DIGITIZATION AND PROCESSING DEVICE

The present invention relates to devices for processing analog and/or digital signals, and more particularly, to integrated circuits that utilize multiple clock frequencies for digitizing and processing various analog and/or digital signals.

Integrated circuits, or ICs, are extensively used in all types of electronic devices. As these electronic devices become more complex, the number of ICs necessary to perform all of the required functions increases and/or the functions of several ICs are combined into a single IC. Even as multiple functions are consolidated into a single IC, it is desirable to reduce the internal complexity of the IC.

Current televisions use many different ICs for processing both analog and digital television signals from various terrestrial and non-terrestrial sources. The next generation of digital/analog televisions, however, will be expected to have even higher levels of integration than current televisions. Higher levels of integration translate into fewer ICs, wherein processes performed by several individual ICs are combined into one IC. However, various obstacles stand in the way of combining processing from analog television signal receivers with those required for digital television signals.

A problem with respect to integration of analog and digital television signal processing ICs is that different sources of video (both analog and digital) may require analog-to-digital (A/D) converters to be run at different sampling rates. Analog television signals are based on line-locked or chroma sub-carrier-locked frequencies, while digitally modulated (digital) television signals are based on their own symbol rates. Also, present A/D technology produces digital crosstalk that adversely affects A/D performance when asynchronous clocks are present.

It is known to use stand-alone digital demodulators using digital interpolation for off-frequency operation. Also, second channel processing for analog signals has been accomplished with an asynchronous sample frequency.

In the latter case, however, the main channel is locked to a parameter of the incoming analog television signal, such as horizontal sync pulses or color burst.

The present invention is a single system IC that performs simultaneous digitization and processing of multiple analog and/or digital signals, using a common frequency source that is not locked to a parameter of the incoming signal. Thus, high performance sampling and processing of all incoming signals may be achieved.

The present invention provides for standard analog video decoding for two channels using a single reference frequency (reference clock) that is not locked to either system. That is, the reference clock is not based on, or locked to, a lockable characteristic of either input signal. Two digital signal processors, for satellite and terrestrial television signals, are modified to perform processing based on the same reference frequency. The present invention provides synchronous frequency operation of all A/Ds and digital signal processors of the multiple channels to prevent erroneous sampling and processing of the incoming signal.

In one form of the invention, a single reference clock of a particular frequency is input to a clock generator that generates all of the operational frequencies (clock signals) needed by the A/D converters and decoding circuitry/logic on the IC. The reference clock is independent, e.g., is not locked to, any synchronizing characteristic of the input signals.

Since there is only one reference clock from which all the other sampling and processing frequencies are generated, the A/Ds will be able to operate with high performance, up to 10-bit accuracy, with little to no digital noise. This is generally not possible with asynchronous sampling frequencies because "quiet zones", needed for sampling the analog input, no longer exist. However, with the multiple sampling frequencies based on a single reference clock (frequency) of the present invention, these quiet zones between digital transitions are preserved.

One circuitry/logic section of the present IC that processes satellite (digital) broadcast television signals, uses an interpolator to process an incoming signal at an appropriate symbol rate related frequency (e.g. 40 MHz) even though

the actual samples may be taken at a different frequency (e.g. 54 MHz). A similar procedure is used for terrestrial digital or vestigal sideband (VSB) television signals where twice the symbol rate is an appropriate frequency (e.g. 21.54 MHz) while the sampling frequency (clock signal) is greater than the particular frequency (e.g. 27 MHz). Analog television signal processing is also accomplished at a particular frequency (e.g. 18 MHz) for each channel. Even though the analog television signal samples are not locked to the incoming line rate, the horizontal frequency is determined with sub-sample accuracy for each channel. A final sample rate converter has a frequency (e.g. 27 MHz) that corresponds to a frequency for luma (e.g. 13.5 MHz) plus a frequency for each of the color difference signals (e.g. 6.75 MHz). This provides non-jittering lines of data output. Additionally, a chroma demodulator of the present IC uses a digital discrete-time oscillator (DTO) that is locked to the incoming chroma burst signal for each of the incoming signals. Thus, all of the digital processing is achieved using synchronous clocks in spite of the asynchronous character inherent in the various processing sections of circuitry/logic, such as by four types of television signal systems.

The present invention also achieves dual use of much of the digital circuitry in the dual NTSC signal processing section. The digital color decoder (DCD) performs all of the necessary signal processing functions for decoding NTSC video including comb filtering for separating luma and chroma, chroma demodulation for generating the color difference signals, synchronizing (sync) signal separation, sample rate conversion (SRC) to a standard interface frequency, and vertical blanking interval (VBI) data slicing. The VBI typically includes closed caption, "V-chip" parental control/rating information, program guide, teletext data, and the like. All of these functions are included for both the main channel video and the second channel video, which is usually used for picture-in-picture (PIP).

In accordance with another aspect of the present invention, the DCD combines the two channels, duplicating only the actual data storage components required for the two channels, and uses the same circuits for most of the processing by running at twice the required sampling/clock frequency and

switching channels on every clock cycle. Thus, for example, each 18 MHz channel is processed on every other clock cycle at 36 MHz.

In another form, the present invention includes an analog signal processing section and a clock generator. The analog signal processing section is operable to process analog signals having a synchronizing component, such as a horizontal sync pulse or the like. The clock generator is operable to produce internal clocking signals based on an external reference signal for use by the analog signal processing section, wherein the external reference signal is independent of the synchronizing component of the analog signals.

In another form, the present invention includes an analog signal processing section, a digital signal processing section, a first A/D converter associated with the analog signal processing section, and a second A/D converter associated with the digital signal processing section. The integrated circuit further includes a clock generator operable to provide first and second clock signals for the first and second analog-to-digital converters respectively from a single reference clock signal, wherein the first and second clock signals provide synchronous operation of the first and second analog-to-digital converters.

In yet another form, the present invention includes an analog signal processing section, a digital signal processing section, and a clock generator. The clock generator is operable to produce multiple clock signals of different frequencies for use by the analog and digital processing sections, wherein the clock generator uses a single reference clock signal of a given frequency that is independent of any synchronizing characteristic of the input analog and/or digital signal. The analog and digital signal processing sections process their respective analog and digital signals simultaneously.

The present invention is described with reference to the accompanying drawings, wherein:

Fig. 1 is a block diagram of an exemplary system in which the present IC may be used;

Fig. 2 is a block diagram of the IC used in the exemplary system of Fig. 1, incorporating an embodiment of the present invention;

Fig. 3 is a chart showing the various digital frequencies used in the IC of Fig. 2;

Fig. 4 is a block diagram of the digital color decoder of the IC of Fig. 2; and

Fig. 5 is a block diagram of a comb filter implementation of the IC of Fig. 2.

Corresponding reference characters indicate corresponding parts throughout the several views.

With reference to Fig. 1 there is depicted a block diagram of a system 10 suitable for using an IC according to the present invention. System 10 comprises a plurality of integrated circuits (ICs) for signal and/or data and information processing, wherein at least one IC requires multiple clocks, clock frequencies, or clock/clocking signals for proper functioning. This type of IC may be termed a multiple clock IC. It should be appreciated that system 10 is an exemplary environment/application utilizing the present multiple clock IC. The multiple clock IC of system 10, in accordance with the principles set forth herein, may take many forms and/or perform many functions as is known to those skilled in the art.

In system 10, the multiple clock IC performs television signal processing for a variety of television signal formats from a variety of sources. Briefly, the multiple clock television signal processor IC incorporating the present invention is adapted/operable to process digital satellite television signals, terrestrial (including cable distribution) digital television signals, and terrestrial (including cable distribution) analog television signals. These analog and digital signals may be provided in various encoding schemes and/or modulation schemes.

System 10 includes television signal processing device 12, which may be a television apparatus, a set-top box, or the like (collectively "television apparatus"). Television signal processing device 12 includes processing circuitry/logic 16 for decoding a received television signal. Processing circuitry/logic 16 is operable to decode and process digitally modulated analog audio and video television signals or transmissions ("digital television signals") from Direct Broadcast Satellite (DBS) system 20 modulated using for example,

QPSK (Quadrature Phase Shift Keying) modulation/encoding format. Processing circuitry/logic 16 is also operable to decode and process digital television signals from terrestrial Digital Television (DTV) antenna 26. Such television signals may be digitally modulated using a VSB (Vestigal SideBand) modulation/encoding format.

Processing circuit/logic 16 is also operable, to process analog audio and video television signals ("analog television signals") from terrestrial analog antenna 30 received via a signal path or line 32, as well as analog television signals from CATV (cable television) system 34. The modulation/encoding format of the analog television signals is typically NTSC, but other formats may be used. The processing of analog television signals typically includes digitizing the input signals through appropriate circuitry, software, and/or other components. Digital television signals from CATV system 34 may also be decoded and processed. It should be appreciated that television apparatus 12 is adapted to receive and process analog and/or digital television signals from sources other than that shown.

Television signal processing device 12 also typically includes memory 18, which includes stored program instructions (i.e. software) for controlling the operation of television signal processing device 12. Circuitry/logic 24 is provided for other functionality of television signal processing device 12, which functionality is not necessary for understanding or practicing the present invention, and will not be described in detail.

System 10 also includes display 14 that is coupled to processing circuitry/logic 16, and suitable for displaying the video portion of the television signal (and any OSD thereof). In the case of a set-top box, or the like, display 14 is associated with a display of an attached television set. Output 38 may also be provided to supply audio and/or video from processing device 12 to another device including a video recorder and the like.

Television signal processing device 12 may be an analog/digital television including, but not limited to DTV-320 HDTV (High Definition Television) manufactured by Thomson Consumer Electronics, Inc. of Indianapolis, Indiana, a digital television such as a high definition digital television (HDTV), a set-top box

capable of utilizing analog/digital television signals, a television signal storage device, or any other device that can process various forms of television signals.

In accordance with an aspect of the present invention, at least one of the plurality of ICs in system 10 is a multiple clock IC. The multiple clock IC utilized in processing circuitry/logic 16 of television apparatus 12, is known as a Universal Link IC, and is illustrated in Fig. 2. Universal link IC 40 is an integrated circuit of mixed signal design, i.e. it has both analog and digital television signal processing circuitry, and incorporates, or integrates, several television signal processing functions into a single IC.

Referring to Fig. 2, there is shown a block diagram of Universal Link Universal Link IC 40 used in television apparatus 12. The multiple clock signals of different frequencies are generated by Universal Link IC 40 using a single externally generated reference clock signal of a given frequency. Universal Link IC 40 includes I/O pin 48 that receives the externally generated reference clock signal. In the present embodiment, Universal Link IC 40 uses an externally provided 27 MHz reference clock signal. Other external reference clock signal frequencies may be used in accordance with the principles set forth herein.

Notably, the external reference clock signal is not based on, or locked to, any lockable characteristic, such as a sync pulse or color burst, of an incoming television signal (either analog or digital). Rather, the external reference clock signal is chosen to provide easy multiplication and division thereof for generating clock signals of appropriate frequencies to accommodate the clocking signal frequency requirements of the various sections or blocks of circuitry/logic of Universal Link IC 40.

In Universal Link IC 40, the external reference clock signal is provided to Phase Locked Loop (PLL) synthesizer 50, which produces an output clock signal of a given frequency on output/line 52. Here, the PLL output clock signal is chosen to be 108 MHz and may be considered an internal reference clock signal. All remaining required clock signals are generated from this internal reference clock signal.

The 108 MHz internal reference clock signal is provided to clock generator 54, which contains the appropriate circuitry/logic to generate multiple clock

frequencies. The actual number of clock signals produced by clock generator 54 is dependent upon the clock signal requirements of the particular IC. In Universal Link IC 40, clock generator 54 produces four (4) clock signals of different frequencies and one (1) clock signal of the same frequency as the internal reference clock signal. Each generated clock signal is then routed to the appropriate section or block of circuitry/logic.

In accordance with the present invention, the internal IC reference clock frequency generated by PLL clock synthesizer 50 is a multiple of the external reference clock frequency. More particularly, the internal IC reference clock frequency is preferably a whole number multiple of the external reference clock frequency. The internal IC reference clock frequency is also chosen such that it can be divided into the plurality of IC clock signals or frequencies that are usable by the various sections or blocks of circuitry/logic.

In the present case, the internal reference clock signal frequency is 108 MHz, which is four (4) times the external reference clock signal frequency of 27 MHz. Clock generator 54 then produces a 54 MHz clock signal, which is one-half (1/2) of the 108 MHz internal IC clock signal, a 36 MHz clock signal, which is one-third (1/3) of the 108 MHz internal IC clock signal, a 27 MHz clock signal which is one-fourth (1/4) of the 108 MHz internal IC clock signal and an 18 MHz clock signal which is one-sixth (1/6) of the 108 MHz internal IC clock signal. Therefore, clock generator 54 generates 4 subclocks that are subharmonics of the master internal clock with no phase shift.

Another factor in determining the frequencies of internal clock signals is the sampling rates, or the clocking rates, for the various sections or blocks of circuitry/logic of Universal Link IC 40. As indicated above, Universal Link IC 40 includes three main sections. The three main sections are: "Satlink" section 42, which is operable to receive and demodulate/decode satellite transmitted television signals; "VSB (Vestigal SideBand) link" section 44 which is operable to receive and demodulate/decode terrestrially transmitted general digital and/or digital high definition (HDTV) signals; and "DCD" (Digital Color Decoder) section 46, which is a block of circuitry/logic that is operable to provide switching, chroma demodulation, and other signal processing of NTSC (analog) signals.

Universal Link IC 40 provides several separate decoding/demodulation systems, including a first system for a main analog television signal, a second system for an auxiliary analog television signal (such as PIP or picture-in-picture and/or POP or picture-on-picture), a third system for digital satellite television signals, and a fourth system for digital terrestrial television signals. Sections 42, 44, and 46 operate independently and in parallel. Because of the nature of the various signals, various portions of circuitry/logic of the sections or blocks of circuitry/logic require different clocking or sampling frequencies.

Satlink section 42 accepts an I, Q input into an appropriate "x-bit" A/D converter. In particular, the I and Q inputs are provided to into a dual 6-bit A/D converter 56 that is clocked or sampled using the 54 MHz clock signal. Demodulation block 58 and Forward Error Correction (FEC) block 60 further process the satellite broadcast digital television signal. In particular, demodulation block 58 and FEC block 60 uses an interpolator to process the satellite broadcast (digital) signal at an appropriate symbol rate related frequency for the satellite broadcast digital television signals. In the present case, the appropriate symbol rate frequency is 40 MHz. The dual 6-bit A/D converter 56, however, utilizes the 54 MHz IC clock signal to clock or sample (oversample) the incoming television signal, even though it requires only a 40 MHz clock or sampling signal. The 54 MHz clock provides a thirty-five percent (35%) increase in clock or sampling frequency over the clock or sampling frequency required.

Similar to Satlink section 42, VSB section 44 receives the VSB digital broadcast television signal through an appropriate "x-bit" A/D converter. VSB section 44 receives the VSB signal through 10-bit A/D converter 62 that is clocked with the 27 MHz clock signal. Demodulation block 64, equalizer block 66, phase tracker block 68, and Forward Error Correction (FEC) block 70 further process the terrestrial broadcast digital television signal. In particular, demodulation block 64, equalizer block 66, phase tracker block 68, and FEC block 70 processes the VSB signal at twice a symbol rate related frequency for the VSB (i.e. terrestrial) broadcast digital television signals. In the present case, the appropriate symbol rate frequency is 10.77 MHz, so twice the appropriate symbol rate frequency is 21.54 MHz. The 10-bit A/D converter 62, however,

utilizes the 27 MHz IC clock signal to clock or sample (oversample) the incoming television signal, even though it requires only a 21.54 MHz clock or sampling signal. The 27 MHz clock provides an approximately twenty-five percent (25%) increase in clock or sampling frequency over the sampling frequency required.

In DCD section 46, the analog sampling is accomplished using the 18 MHz clock signal for each channel of the analog television signal. Even though these samples are not locked to a characteristic of the input television signal, this horizontal frequency is determined with sub-sample accuracy for each channel. DCD section 46 is operable to receive two analog television signals (i.e. one for the main channel and the other for the PIP or POP) at DCD analog circuits section 72. The four (4) CV/Y signals thereof are input into switch 74 that appropriately sends the signals to two 10-bit A/D converters 76 and 78. The two sets of separate C, U, and V INS thereof, are input into switch 80 that appropriately sends the signal to two 10-bit A/D converters 82 and 84. The outputs of these four 10-bit A/D converters 76, 78, 82, and 84 are input into dual channel NTSC digital color decoder 86. The final sample rate convertion is accomplished at 27 MHz (sequential 13.5 MHz for luma and 6.75 MHz for each of the color difference signals. This provides non-jittering lines of data output. In addition, the chroma demodulator uses a digital discrete time oscillator (DTO) that is locked to the incoming chroma burst signal for each of the incoming signals.

All of the A/D processing and digital signal processing is accomplished using synchronous clocks in spite of the asynchronous character inherent in these four signaling systems. Also, each IC clock signal frequency generated by clock generator 54 is equal to or greater than the clock/sampling signal frequency required for proper operation of the appropriate portion of the circuitry/logic. Such oversampling may be accommodated for later in the processing of the particular signal. Undesirable effects generated by the synchronous operation of the A/Ds and signal processor sections may be compensated for by the chroma demodulation sections 102 and 104, and SRC and synch processors 110 and 112. The techniques for removing such effects are well known to those skilled in the art and will not be discussed in detail here.

Since there is only one reference clock signal from which all of the other sampling and processing frequencies are generated, the A/Ds will be able to operate with high performance (i.e. up to 10-bit accuracy) and have little to no digital noise. This not possible with asynchronous sampling frequencies because the "quiet zones" needed for sampling the analog signal no longer exist. However, with multiple sampling frequencies based on the same clock, the quiet zones between digital transitions are preserved. (see Fig. 3).

Another aspect of the present invention is the dual use of portions of the digital circuitry for processing NTSC television signals. In this regard, reference is made to Fig. 4, which depicts a block diagram of DCD block 86. DCD block 86 performs all of the necessary signal processing functions for two NTSC (analog) television signals. DCD block 86 includes dual comb filters 90 and 92 for separating luma and chroma from the two incoming analog television signals which are input into respective luma and chroma switches 94 and 96. The respective luma and chroma switches 94 and 96 are each clocked at 36 MHz (twice the required frequency of 18 MHz for a single channel) such that each channel's chroma and luma components are switched on every clock. Thus, each 18 MHz channel is processed on every other clock cycle at 36 MHz.

The chroma components are input to respective ACC and chroma demodulation blocks 102 and 109. The UV components are meanwhile forwarded to demultiplexers 98 and 100 to obtain respective, separate U and V components. The U and V outputs of the chroma demodulation modules 102 and 104 (color difference signals) are combined with the U and V outputs of the respective demultiplexers 98 and 100 in respective UV switches 106 and 108, which again are clocked at 36 MHz (twice the required frequency of 18 MHz for a single channel) such that each channel's chroma and luma components are switched on every clock. Thus, each 18 MHz channel is processed on every other clock cycle at 36 MHz.

The luma and UV components are forwarded to respective sample rate converters and synchronizing (sync) signal separation blocks 110 and 112 to produce a signal having a standard interface frequency. Additionally, vertical blanking interval (VBI) data slicing is accomplished by data slicers 114 and 116

wherein closed caption, "v-chip" parental control information, teletext data, program guide information, and the like, is obtained. Outputs of the respective sample rate converters and sync processors 110 and 112, and the respective data slicers 114 and 116 are input to video processor 118 to supply the main channel video and second (auxiliary) channel video. The second channel video is typically used for PIP or POP. As noted earlier, undesirable effects of using a single reference clock are compensated for in chroma demodulation sections 102 and 104, and SRC and sync processors 110 and 112.

With reference to Fig. 5, there is shown a block diagram, generally designated 130, of the comb filter implementation with dual use of much of the logic circuits of DCD block 86 in accordance with an aspect of the present invention. The first composite video of a clocking or sampling frequency of 18 MHz is input into a data storage device 134 holding one line of the video and into a comb filter 132. At the same time, the second composite video of a clocking or sampling frequency of 18 MHz is input into a data storage device 136 holding one line of the video and into the comb filter 132. Data storage devices 134 and 136 are each clocked at the sampling rate of 18 MHz. Comb filter 132 is clocked at twice 18 MHz or at 36 MHz. In this manner, comb filter 132 alternatively processes the output of data storage devices 134 and 136.

Thus, instead of two completely different circuits, DCD block 86 combines the two channels, duplicating only the actual data storage components. DCD block 86 also uses the same circuits for most of the processing by operating at twice the required frequency and switching channels on every clock.

While this invention has been described as having a preferred design and/or configuration, the present invention can be further modified within the spirit and scope of this disclosure. This application is therefore intended to cover such departures from the present disclosure as come within known or customary practice in the art to which this invention pertains and which fall within the limits of the appended claims. In particular, the present invention is applicable to other circuits where there are prerequisites to operate systems with different frequency requirements, where it is desired to operate the systems/circuits on the same

silicon space, especially those with A/Ds and other analog circuits, in addition to the digital circuitry/logic.

CLAIMS

1. An integrated circuit comprising:

a signal input for receiving an analog signal having a synchronizing characteristic;

a clock input for receiving an external reference clock signal;

a clock generator, coupled to the clock input, for producing a plurality of internal clock signals based on the external reference clock signal; and

a signal processing section, coupled to the signal input and the clock generator, for processing the analog signal in accordance with an appropriate signal standard, the signal processing section having circuitry/logic that are clocked by respective ones of the plurality of internal clock signals, characterized in that

the external reference clock is independent of the synchronizing characteristic of the analog signal, whereby the circuitry/logic are clocked by respective ones of the plurality of internal clock signals, which are independent of the synchronizing characteristic of the input analog signal.

2. The integrated circuit of claim 1, characterized in that the signal processing section includes a plurality of analog to digital (A/D) converters and decoding circuitry/logic, wherein both the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of internal clock signals.

3. The integrated circuit of claim 1, characterized in that the signal processing section is adapted to process two separate analog signals, each of the two separate analog signals having respective synchronizing characteristics, and the external reference clock signal is independent of the synchronizing characteristics.

4. The integrated circuit of claim 3, characterized in that the analog signal processing section processes the two separate analog signals using a single processing channel, the single processing channel being clocked by an internal clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the analog signals.

5. The integrated circuit of claim 4, characterized in that the analog signals are television signals.

6. The integrated circuit of claim 5, characterized in that the synchronizing characteristic includes one of a horizontal sync pulse and a color burst signal.

7. The integrated circuit of claim 1, characterized in that the signal processing section is further operable to process a digital input signal having a synchronizing characteristic, and the external reference clock signal is independent of the synchronizing characteristic of the digital input signal.

8. The integrated circuit of claim 7, characterized in that the synchronizing characteristic of the digital input signal is the symbol rate.

9. A television apparatus, comprising:

a signal input for receiving an input signal, the input signal having a synchronizing characteristic;

a clock signal generator for producing a reference clock signal;

a signal processor, coupled to the signal input and the clock signal generator, having circuitry/logic for processing the input signal in accordance with an appropriate signal standard and providing an output signal suitable for display on a display device, the signal processor generating a plurality of internal clock signals based on the reference clock signal; and

an signal output, coupled to the signal processor, for receiving and coupling the output signal to a display device, characterized in that

the reference clock signal is independent of the synchronizing characteristic of the input signal, and the circuitry/logic of the signal processor are clocked by respective ones of the plurality of internal clock signals, which are independent of the synchronizing characteristic of the input signal.

10. The television apparatus of claim 9, characterized in that the signal processing section includes a plurality of analog to digital (A/D) converters and decoding circuitry/logic, wherein both the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of internal clock signals.

11. The television apparatus of claim 10, characterized in that the signal processing section is adapted to process two separate analog signals, each of the two separate analog signals having respective synchronizing characteristics, and the reference clock signal is independent of the synchronizing characteristics.

12. The television apparatus of claim 11, characterized in that the analog signal processing section processes the two separate analog signals using a single processing channel, and the single processing channel is clocked by an internal clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the analog signals.

13. The television apparatus of claim 12, characterized in that the synchronizing characteristics include one of a horizontal sync pulse and a color burst signal.

14. The television apparatus of claim 9, characterized in that the signal processing section is further operable to process a digital input signal having a synchronizing characteristic, the external reference clock signal is independent of the synchronizing characteristic of the digital input signal, and the synchronizing characteristic is the symbol rate.

15. A method for processing input signals having synchronizing components, the method comprising the steps of:

receiving an input signal having a synchronizing component;

generating a reference clock signal;

generating a plurality of internal clock signals based on the reference clock signal;

converting the analog input signal into a digital signal using analog to digital (A/D) converters that are clocked using one of the plurality of internal clock signals; and

decoding the converted digital signal in accordance with an appropriate television signal standard using decoding circuitry/logic to provide an output signal suitable for display, the decoding circuitry/logic being clocked by at least one of the plurality of internal clock signals, characterized in that

the reference clock signal is generated independently of the synchronizing component, wherein both the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of internal clock signals, which are independent of the synchronizing characteristic of the input signal.

16. The method according to claim 15, characterized in that

the receiving step comprises receiving two analog input signals, each having a respective synchronizing characteristic,

the converting step comprises converting the two analog input signals to respective digital signals, and

the decoding step comprises decoding the two digital signals to provide two output signal using a single processing channel that is clocked by an internal clock signals that has a frequency of at least twice the required clocking speed necessary for processing a single analog signal.

17. The method according to claim 15, characterized in that

the receiving step further comprises receiving a digital input signal having a synchronizing characteristic, and

the decoding step further comprises decoding the digital input signal using decoding circuitry/logic that is clocked by a respective one of the internal clock signals that is independent of the synchronizing characteristic of the digital input signal.

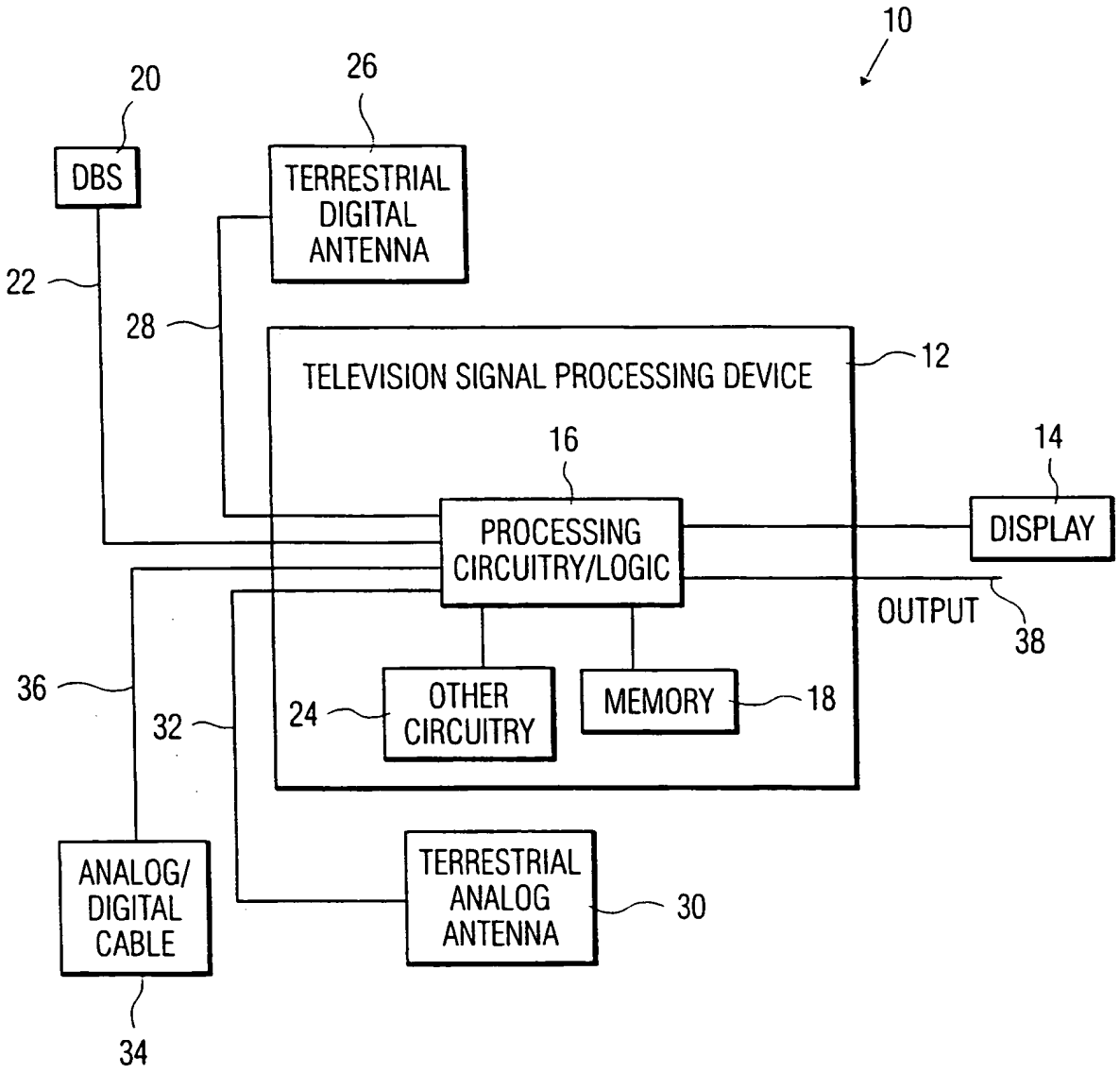
10
20
26
DBS
TERRESTRIAL DIGITAL ANTENNA
22
28
TELEVISION SIGNAL PROCESSING DEVICE
12
16
14
PROCESSING CIRCUITRY/LOGIC
DISPLAY
OUTPUT
38
36
32
24
OTHER CIRCUITRY
MEMORY
18
ANALOG/ DIGITAL CABLE
TERRESTRIAL ANALOG ANTENNA
30
34

FIG. 1

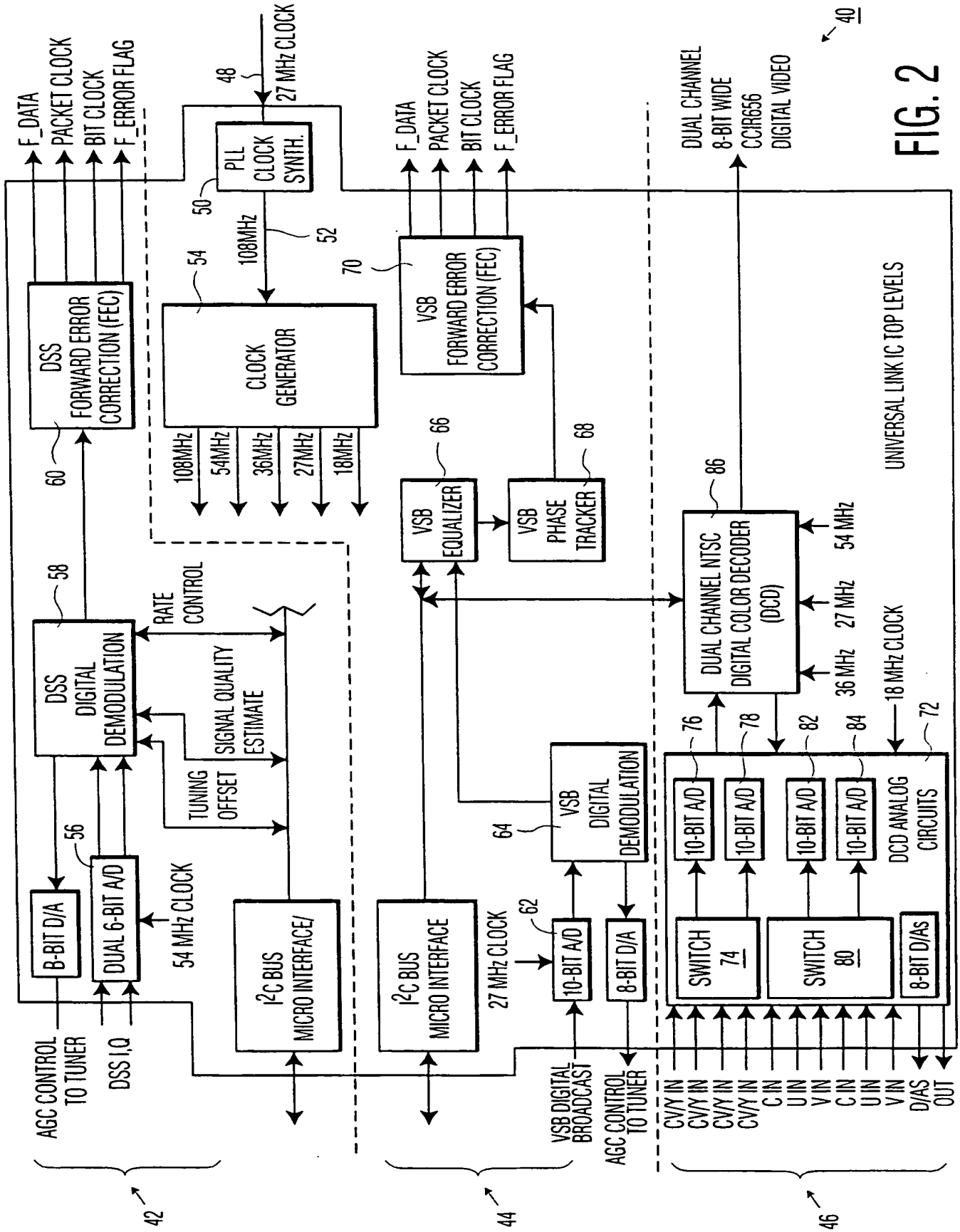
40
F_DATA
PACKET CLOCK
BIT CLOCK
F_ERROR FLAG
48
27 MHz CLOCK
PLL CLOCK SYNTH.
50
108MHz
52
54
CLOCK GENERATOR
108MHz
54MHz
36MHz
27MHz
18MHz
60
DSS FORWARD ERROR CORRECTION (FEC)
70
VSB FORWARD ERROR CORRECTION (FEC)
66
VSB EQUALIZER
68
VSB PHASE TRACKER
58
DSS DIGITAL DEMODULATION
RATE CONTROL
SIGNAL QUALITY ESTIMATE
TUNING OFFSET
56
B-BIT D/A
DUAL 6-BIT A/D
54 MHz CLOCK
I2C BUS MICRO INTERFACE/
AGC CONTROL TO TUNER
DSS I,Q
64
VSB DIGITAL DEMODULATION
62
10-BIT A/D
8-BIT D/A
I2C BUS MICRO INTERFACE
27 MHz CLOCK
VSB DIGITAL BROADCAST
AGC CONTROL TO TUNER
DUAL CHANNEL 8-BIT WIDE CCIR656 DIGITAL VIDEO
86
DUAL CHANNEL NTSC DIGITAL COLOR DECODER (DCD)
54 MHz
27 MHz
36 MHz
18 MHz CLOCK
UNIVERSAL LINK IC TOP LEVELS
76
78
82
84
72
10-BIT A/D
10-BIT A/D
10-BIT A/D
10-BIT A/D
DCD ANALOG CIRCUITS
SWITCH 74
SWITCH 80
8-BIT D/As
CV/Y IN
CV/Y IN
CV/Y IN
CV/Y IN
C IN
U IN
V IN
C IN
U IN
V IN
D/AS OUT
42
44
46

FIG. 2

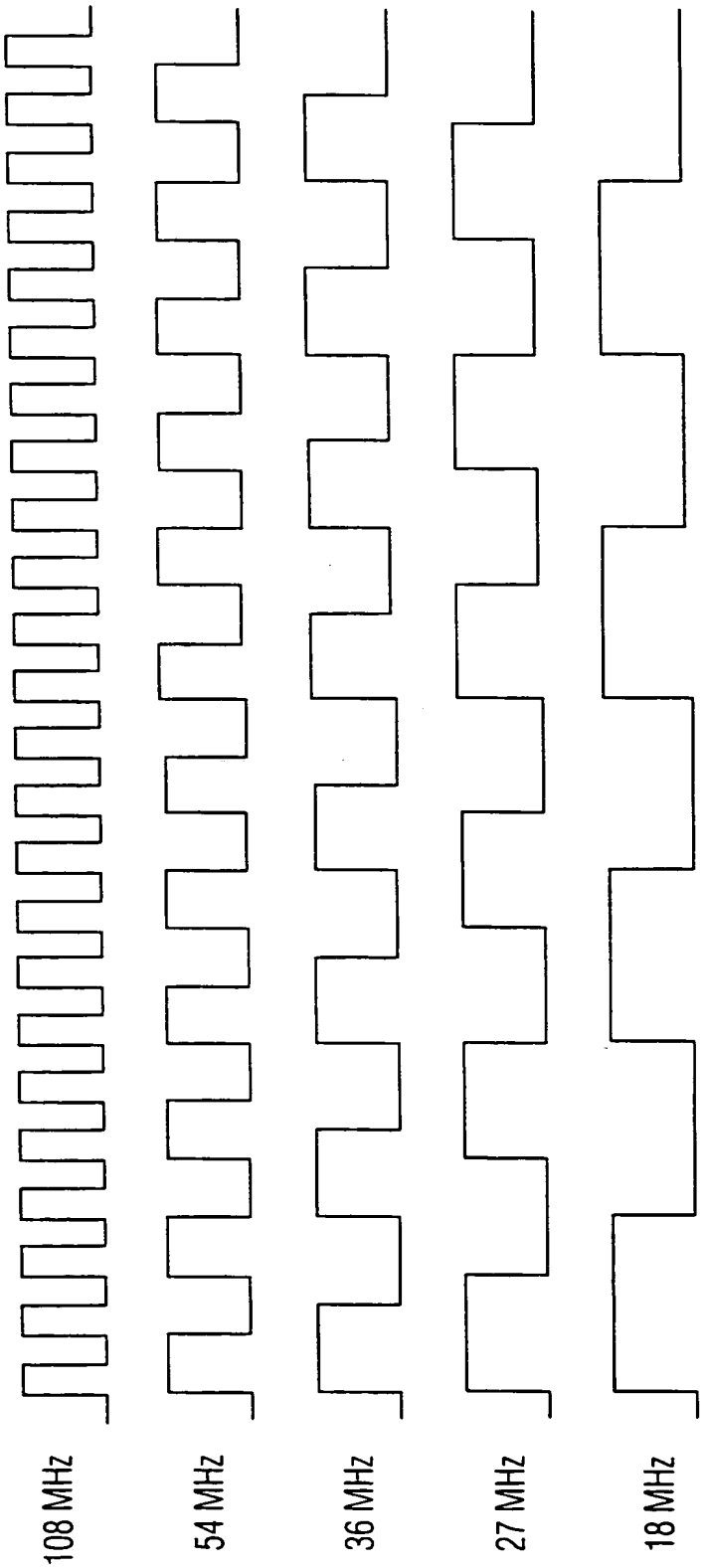

FIG. 3

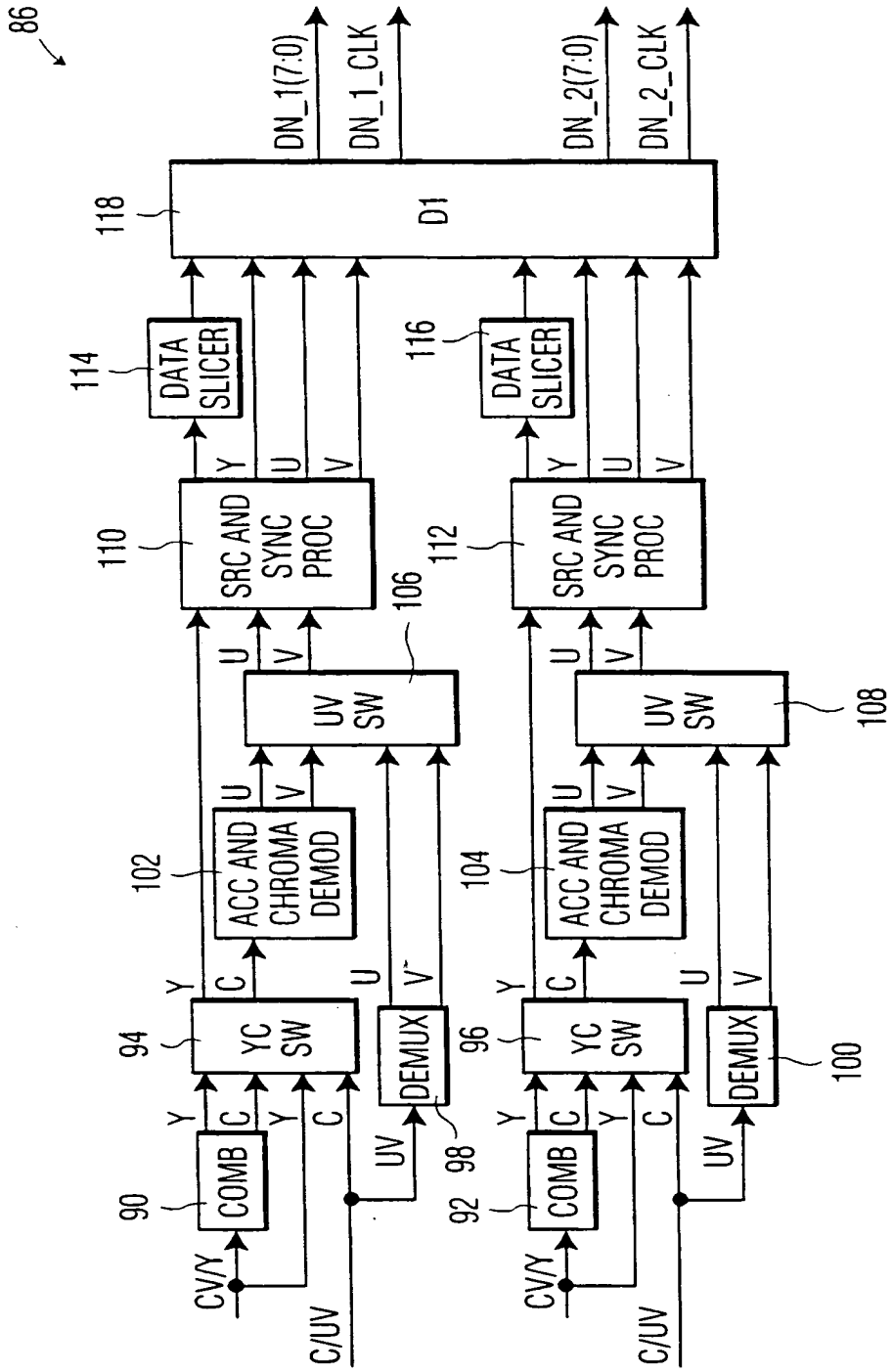
86
DN_1(7:0)
DN_1_CLK
DN_2(7:0)
DN_2_CLK
118
D1
114
DATA SLICER
116
DATA SLICER
110
SRC AND SYNC PROC
112
SRC AND SYNC PROC
106
UV SW
108
UV SW
102
ACC AND CHROMA DEMOD
104
ACC AND CHROMA DEMOD
94
YC SW
96
YC SW
DEMUX
100
DEMUX
98
90
COMB
92
COMB
CV/Y
C/UV
Y
C
U
V

FIG. 4

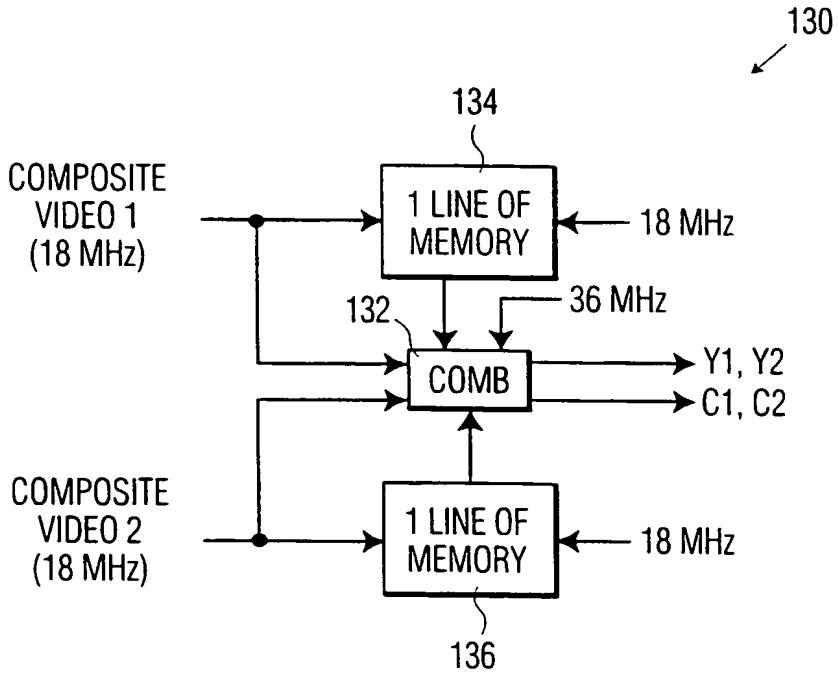
130
134
COMPOSITE VIDEO 1 (18 MHz)
1 LINE OF MEMORY
18 MHz
36 MHz
132
COMB
Y1, Y2
C1, C2
COMPOSITE VIDEO 2 (18 MHz)
1 LINE OF MEMORY
18 MHz
136

FIG. 5

INTERNATIONAL SEARCH REPORT

Int. Application No
PCT/US 00/28059

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N9/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 98 46027 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 15 October 1998 (1998-10-15) page 1, line 6 - line 18 page 3, line 16 -page 4, line 9 ---	1-6,9-13
A	US 5 367 337 A (PYLE HARRY S ET AL) 22 November 1994 (1994-11-22) column 2, line 16 - line 34 column 4, line 14 - line 30 column 9, line 20 -column 10, line 15 ---	1-6
A	WO 99 46931 A (GEN INSTRUMENT CORP) 16 September 1999 (1999-09-16) page 5, line 5 - line 18 page 6, line 26 -page 7, line 14 page 21, line 1 - line 18 page 26, line 4 -page 27, line 3 ---	1,9,15

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 February 2001	08/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Berwitz, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

In. Application No
PCT/US 00/28059

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 808 691 A (MALCOLM JR RONALD D ET AL) 15 September 1998 (1998-09-15) column 1, line 21 - line 31	1,15

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

In Application No
PCT/US 00/28059

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 9846027	A	15-10-1998	EP	0906701 A	07-04-1999
			JP	2000511747 T	05-09-2000
			US	6064446 A	16-05-2000
US 5367337	A	22-11-1994	NONE		
WO 9946931	A	16-09-1999	US	6147713 A	14-11-2000
			AU	2796099 A	27-09-1999
			EP	1062806 A	27-12-2000
US 5808691	A	15-09-1998	US	6052152 A	18-04-2000

REPLACED BY ART 34 AMDT

CLAIMS

1. An integrated circuit comprising:

a signal input for receiving an analog signal having a synchronizing characteristic;

a clock input for receiving an external reference clock signal;

a clock generator, coupled to the clock input, for producing a plurality of internal clock signals based on the external reference clock signal; and

a signal processing section, coupled to the signal input and the clock generator, for processing the analog signal in accordance with an appropriate signal standard, the signal processing section having circuitry/logic that are clocked by respective ones of the plurality of internal clock signals, characterized in that

the external reference clock is independent of the synchronizing characteristic of the analog signal, whereby the circuitry/logic are clocked by respective ones of the plurality of internal clock signals, which are independent of the synchronizing characteristic of the input analog signal.

2. The integrated circuit of claim 1, characterized in that the signal processing section includes a plurality of analog to digital (A/D) converters and decoding circuitry/logic, wherein both the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of internal clock signals.

3. The integrated circuit of claim 1, characterized in that the signal processing section is adapted to process two separate analog signals, each of the two separate analog signals having respective synchronizing characteristics, and the external reference clock signal is independent of the synchronizing characteristics.

4. The integrated circuit of claim 3, characterized in that the analog signal processing section processes the two separate analog signals using a single processing channel, the single processing channel being clocked by an internal clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the analog signals.

5. The integrated circuit of claim 4, characterized in that the analog signals are television signals.

6. The integrated circuit of claim 5, characterized in that the synchronizing characteristic includes one of a horizontal sync pulse and a color burst signal.

7. The integrated circuit of claim 1, characterized in that the signal processing section is further operable to process a digital input signal having a synchronizing characteristic, and the external reference clock signal is independent of the synchronizing characteristic of the digital input signal.

8. The integrated circuit of claim 7, characterized in that the synchronizing characteristic of the digital input signal is the symbol rate.

9. A television apparatus, comprising:

a signal input for receiving an input signal, the input signal having a synchronizing characteristic;

a clock signal generator for producing a reference clock signal;

a signal processor, coupled to the signal input and the clock signal generator, having circuitry/logic for processing the input signal in accordance with an appropriate signal standard and providing an output signal suitable for display on a display device, the signal processor generating a plurality of internal clock signals based on the reference clock signal; and

an signal output, coupled to the signal processor, for receiving and coupling the output signal to a display device, characterized in that

the reference clock signal is independent of the synchronizing characteristic of the input signal, and the circuitry/logic of the signal processor are clocked by respective ones of the plurality of internal clock signals, which are independent of the synchronizing characteristic of the input signal.

10. The television apparatus of claim 9, characterized in that the signal processing section includes a plurality of analog to digital (A/D) converters and decoding circuitry/logic, wherein both the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of internal clock signals.

11. The television apparatus of claim 10, characterized in that the signal processing section is adapted to process two separate analog signals, each of the two separate analog signals having respective synchronizing characteristics, and the reference clock signal is independent of the synchronizing characteristics.

12. The television apparatus of claim 11, characterized in that the analog signal processing section processes the two separate analog signals using a single processing channel, and the single processing channel is clocked by an internal clock signal that has a signal frequency of at least twice the required clocking speed necessary for processing a single one of the analog signals.

13. The television apparatus of claim 12, characterized in that the synchronizing characteristics include one of a horizontal sync pulse and a color burst signal.

14. The television apparatus of claim 9, characterized in that the signal processing section is further operable to process a digital input signal having a synchronizing characteristic, the external reference clock signal is independent of the synchronizing characteristic of the digital input signal, and the synchronizing characteristic is the symbol rate.

15. A method for processing input signals having synchronizing components, the method comprising the steps of:

receiving an input signal having a synchronizing component;

generating a reference clock signal;

generating a plurality of internal clock signals based on the reference clock signal;

converting the analog input signal into a digital signal using analog to digital (A/D) converters that are clocked using one of the plurality of internal clock signals; and

decoding the converted digital signal in accordance with an appropriate television signal standard using decoding circuitry/logic to provide an output signal suitable for display, the decoding circuitry/logic being clocked by at least one of the plurality of internal clock signals, characterized in that

the reference clock signal is generated independently of the synchronizing component, wherein both the A/D converters and the decoding circuitry/logic are clocked by respective ones of the plurality of internal clock signals, which are independent of the synchronizing characteristic of the input signal.

16. The method according to claim 15, characterized in that

the receiving step comprises receiving two analog input signals, each having a respective synchronizing characteristic,

the converting step comprises converting the two analog input signals to respective digital signals, and

the decoding step comprises decoding the two digital signals to provide two output signal using a single processing channel that is clocked by an internal clock signals that has a frequency of at least twice the required clocking speed necessary for processing a single analog signal.

17. The method according to claim 15, characterized in that

the receiving step further comprises receiving a digital input signal having a synchronizing characteristic, and

the decoding step further comprises decoding the digital input signal using decoding circuitry/logic that is clocked by a respective one of the internal clock signals that is independent of the synchronizing characteristic of the digital input signal.

INTERNATIONAL SEARCH REPORT

International Application No
[redacted]/US 00/28059

A. CLASSIFICATION OF SUBJECT MAT[redacted]
IPC 7 H04N9/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 98 46027 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 15 October 1998 (1998-10-15) page 1, line 6 - line 18 page 3, line 16 -page 4, line 9 ---	1-6,9-13
A	US 5 367 337 A (PYLE HARRY S ET AL) 22 November 1994 (1994-11-22) column 2, line 16 - line 34 column 4, line 14 - line 30 column 9, line 20 -column 10, line 15 ---	1-6
A	WO 99 46931 A (GEN INSTRUMENT CORP) 16 September 1999 (1999-09-16) page 5, line 5 - line 18 page 6, line 26 -page 7, line 14 page 21, line 1 - line 18 page 26, line 4 -page 27, line 3 --- -/--	1,9,15

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 February 2001	08/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Berwitz, P

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
P[redacted]/US 00/28059

C.(Continuation) DOCUMENTS CONSIDE[redacted]O BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 808 691 A (MALCOLM JR RONALD D ET AL) 15 September 1998 (1998-09-15) column 1, line 21 - line 31	1,15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/28059

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 9846027	A	15-10-1998	EP	0906701 A	07-04-1999
			JP	2000511747 T	05-09-2000
			US	6064446 A	16-05-2000
US 5367337	A	22-11-1994	NONE		
WO 9946931	A	16-09-1999	US	6147713 A	14-11-2000
			AU	2796099 A	27-09-1999
			EP	1062806 A	27-12-2000
US 5808691	A	15-09-1998	US	6052152 A	18-04-2000